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(54) Patterning of porous silicon using silicon carbide mask

(57) A method of selectively forming porous silicon regions (106) in a silicon substrate (100). A masking layer (104) of SiC is deposited by PECVD over the substrate (100) using an organosilicon precursor gas such as trimethylsilane, silane/methane, or tetramethylsilane at a temperature between 200 - 500°C. The masking layer (104) of SiC is then patterned and etched to expose the region of the substrate (100) where porous silicon is desired. An anodization process is performed to convert a region of the substrate to porous silicon (106). The SiC masking layer (104) withstands the HF electrolyte of the anodization process with little to no degradation.

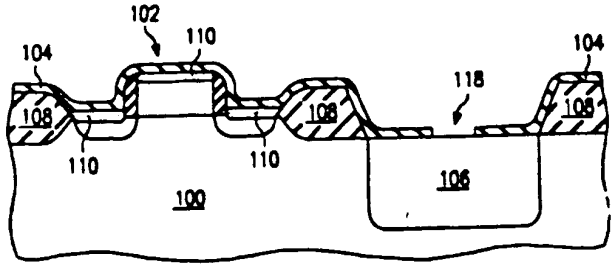

FIG. 3H

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Description

FIELD OF THE INVENTION

[0001] The invention is generally related to the field of forming porous silicon areas in semiconductor devices and more specifically to patterning techniques for forming such porous silicon areas.

BACKGROUND OF THE INVENTION

[0002] Porous silicon (PS) has a low dielectric constant and high resistivity which make it useful for various applications. Some reported applications include: isolation of power devices from other circuitry and optoelectronics/photoluminesence. PS is formed by anodic oxidation of a silicon wafer in a solution of hydrofluoric acid and methanol. Uniform, thick (100 μm) films having a specular surface can be produced in 15 minutes. The PS film structure consists of interconnected pores in a single crystal silicon matrix which retains the orientation of the silicon wafer. The pore fraction is a function of the anodization conditions and typically ranges from 30% to 50%.

[0003] The pore structure of PS is determined by the doping level of the starting silicon wafer. In degeneratively doped n-type or p-type silicon, the structure consists of many long pores running perpendicular to the silicon wafer surface with many small "buds" on the sides of the pores which can result in branching. In lightly doped n-type or p-type silicon, the pore structure consists of an apparently random, interconnected distribution of voids. For a pore fraction of 50%, the size of the pores in lightly doped material is in the 50Å range, while those in degeneratively doped material are around 150 Å. Once the sidewalls of a pore have formed, they are remarkably resistant to further anodic attack. At the start of anodization, inhomogenities in the region of the semiconductor-electrolyte interface result in localization of the current flow and the initiation of pores. The silicon between the pores is depleted and is therefore highly resistive (> 10^5 Ohm/cm) compared with the electrolyte and the bulk silicon. This results in preferential current flow down the electrolyte in the pores causing the reaction to occur only at the pore tips.

[0004] The construction of a commonly employed chamber is illustrated in FIG. 1. The silicon wafer 10 separates the front 12 and rear 14 half cells, each having a platinum electrode 16 and pumped supply of electrolyte 18. The PS film forms on the anode side of the wafer; the silicon is cathodic in the back half cell and does not react. The most important variables affecting the PS structure are (1) substrate doping type and level; (2) HF concentration (10 - 48%); and (3) current density (typically 1 - 100 mA/cm^2). For a fixed substrate resistivity, similar film porosity can be produced using various combinations of HF concentration and current density. Porosity generally increases with increasing current density and decreasing HF concentration. Porous silicon has a high internal surface area, but the impurities found on these surfaces (oxygen, carbon, fluorine, and hydrogen) should not represent a significant problem for subsequent front-end processing.

[0005] Selective anodization has been demonstrated using various masking materials. Two approaches have been used to define the PS regions: (1) ion irradiation to inhibit anodization and (2) conventional photolithography combined with various masking layers. The use of ion irradiation damages the single crystal silicon regions; this damage must be removed by subsequent processing. For conventional photolithography and masking layers, it is difficult to find a masking material that will not erode in the presence of the HF during the anodization process, which may last on the order of 15 minutes, and that is compatible with standard processing. Several masking materials have been proposed. These include silicon nitride, MOCVD GaAs, RTCVD SiC, and LPCVD SiC. It is not clear whether silicon nitride of reasonable thickness can withstand HF for the duration required for thick porous silicon regions. While GaAs and SiC can withstand HF, the proposed MOCVD GaAs, RTCVD SiC, and LPCVD SiC processes occur at high temperatures (600 - 1300°C). These high temperatures present process integration problems. Therefore, a selective anodization process that is compatible with high volume production remains to be demonstrated.

SUMMARY OF THE INVENTION

[0006] A method of selectively forming porous silicon regions in a silicon substrate is disclosed herein. A layer of SiC is deposited by PECVD over the substrate using a silane/methane, trimethylsilane, tetramethylsilane or other organosilicon precursor gas at a temperature between 200 - 500°C. The layer of SiC is then patterned and etched to expose the region of the substrate where porous silicon is desired. An anodization process is performed to convert a region of the substrate to porous silicon.

[0007] This provides a low temperature process for selectively forming porous silicon regions, and a masking material that is compatible with the anodization processes and is not removed by the HF used in the anodization process.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The present invention will now be further described, by way of example, with reference to the accompanying drawings in which:

FIG. 1 is a schematic of a prior art anodization cell used to form porous silicon layers;

FIG. 2 is a cross-sectional diagram of a substrate having a SiC masking layer according to the invention;

FIGs. 3A-3J are cross-sectional diagrams of a substrate having porous silicon areas according to a first embodiment of the invention at various stages of fabrication; and

FIGs. 4A-4H are cross-sectional diagrams of a substrate having porous silicon areas according to a second embodiment of the invention at various stages of fabrication.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0009] A process is disclosed herein for selectively forming areas of porous silicon in a substrate after the formation of transistors in the substrate. As such, these teachings are believed to be very beneficial for RF (radio frequency) applications by isolating passive RF components from the substrate both in an IC and an integrated Si PC board as will be discussed herein below.

[0010] The production of porous silicon (PS) involves a wet anodic etch process in a bath of a very acidic electrolyte. The electrolyte is typically a combination of HF, H2O, and a surfactant such as ethanol or methanol. The pH level is often less than 1. For selective PS formation, a masking step is necessary to prevent previously grown structures (i.e., transistors) from being removed from the surface during anodization.

[0011] The key aspect of these teachings is in the choice and formation of the masking layer. The problem is that typical masking materials such as photoresist and silicon nitride have poor stability in the presence of HF. To alleviate this problem silicon carbide (SiC) is deposited using a new process that is compatible with production-level IC processing.

[0012] Fig. 2 shows a cross-section of a substrate 100 having transistors 102 formed therein. A masking layer 104 is located over the substrate 100 and transistors 102 except in areas where PS 106 is desired. Masking layer 104 comprises an amorphous-SiC:H layer deposited using an organosilicon gas such as silane/methane, trimethylsilane, or tetramethylsilane, PECVD (plasma-enhanced chemical vapor deposition). Masking layer 104 is carbon rich and a 500Å thick film can withstand an HF electrolyte environment for at least 18 hrs without observable degradation. Substrate temperatures need not exceed 350°C and are typically between 250°C and 350°C depending on the desired film properties. The deposition rate is greater than 200 Å/min with good step coverage. Film stress can be adjusted from -100 to +200 MPa by varying the ambient pressure. Thus, a masking layer comprising an amorphous-SiC:H layer deposited using an organosilicon precursor gas PECVD process overcomes problems with other prior art masking materials of withstanding the HF environment and, by using lower deposition temperatures, overcomes process integration problems with prior art SiC deposition processes.

[0013] A process for forming selective PS areas according to a first embodiment will now be discussed in further detail. In this embodiment, the SiC masking layer 104 is deposited after the transistor silicide process and is not removed from the regions through which contacts will be made. Referring to FIG. 3A, the device is processed through isolation regions 108 and transistor 102 formation. Transistors 102 are fabricated through silicide 110 formation and anneal (Ti or W). Isolation regions 108 are shown as field oxide regions. However, they may alternatively be another type of isolation such as shallow trench isolation STI. For STI, process through STI planarization and etch the polish stop layer, leaving the underlying oxide layer.

[0014] If desired an optional oxide layer (not shown) may be deposited at this point. This oxide layer may be deposited by, for example, PETEOS or LPCVD TEOS to a thickness on the order of 5000 - 10,000Å (Angstroms).

[0015] Next, a resist layer 112 is formed over the surface as shown in FIG. 3B. The resist layer 112 is patterned as shown in FIG. 3C to expose an area 114 of isolation region 108. Area 114 is located over the desired PS site. Then, the oxide of isolation regions 108 is etched leaving sloped sidewalls on the order of 45°, as shown in FIG. 3D. This may, for example, be accomplished in one of the following two ways: (1) isotropic plasma etch using CF_4/O_2 or its equivalent or (2) HF deglaze. Resist layer 112 is then removed using standard ash/cleanup processes.

[0016] It will be apparent to those of ordinary skill in the art that the above oxide pattern and etch steps may alternatively be performed prior to transistor formation.

[0017] A p+ diffusion of boron or similar dopant may be performed prior to the transistor formation to convert the p- epi to p+ w/resistivity on the order of 0.01Ω-cm. If necessary, a deglaze to remove the boron or similar dopant contaminated oxide is then performed and a pad oxide is re-grown to a thickness on the order of 100-500Å.

[0018] Referring to FIG. 3E, a masking layer 104 of a-SiC:H is deposited over the structure. Layer 104 may typically have a thickness in the range of 1000Å to 5000Å. The following process may be used: PECVD using silane/methane, trimethylsilane, tetramethylsilane or other organosilicon precursor gas and Ar or He as carrier gas. The pressure may be on the order of 5 Torr. The gas flow may be in the range of 500-5000 sccm. RF power density may be on the order of 2 W/cm^2 (13.56 MHz). The substrate temperature may be in the range of 200 - 500 °C. If desired, a double deposition step (using the same conditions) may be used to reduce defects.

[0019] Next, a second resist mask 116 is formed over the SiC masking layer 104. Second resist mask 116 exposes a portion 118 of SiC masking layer 104 approximately in the center of where the PS region is desired, as shown in FIG. 3F. The exposed portion 118 is significantly smaller than the width of the desired PS region. The relationship between the size of portion 118 and the desired PS region is optimized based on the PS for-

mation process parameters.

[0020] Referring to FIG. 3G, the exposed portion 118 of SiC masking layer 104 is removed. Methods for removing SiC are known in the art. The following are some exemplary methods for removing portion 118 of SiC masking layer 104. (1) Cl_2 based etch [Selectivity of the etch, with this gas, down to the oxide should not be an issue. Removal rate for SiC relative to SiO_2 of 10:1 has been achieved.] using a chamber pressure: ~300 mTorr (gas flow 10 - 50 sccm) and RF Power density ~0.5 - 1 W/cm^2 (13.56 MHz); (2) $CF_4/O_2/H_2$ based etch using an O_2 fraction 0 - 90%, H_2 flow 0 - 20 sccm, (fluorinated-O_2 gas flow 10 - 50 sccm), chamber pressure; ~10 - 50 mTorr, and RF Power density ~0.5 - 1 W/cm^2 (13.56 MHz); (3) $SF_6/O_2/H_2$ based etch using O_2 fraction 0 - 90%, H_2 flow 0 - 20 sccm, (fluorinated-O_2 gas flow 10 - 50 sccm), chamber pressure; ~10 - 50 mTorr, and RF Power density ~0.5 - 1 W/cm^2 (13.56 MHz); and (4) $CHF_3/CF_4/Ar/O_2/H_2$ based etch using an O_2 fraction 0 - 50%, H_2 flow 0 - 100 sccm, (fluorinated-Ar gas flow 50 - 200 sccm), chamber pressure: ~10 - 50 mTorr, and RF Power density ~0.5 - 1 W/cm^2 (13.56 MHz). Second resist layer 118 is then removed.

[0021] Next, the PS regions 106 are formed by anodization, as shown in FIG. 3H. The thickness of PS region 106 may vary between 10 μm and perhaps the wafer thickness, depending on the application. Typically, PS region 106 may be in the range of 10 - 200 μm. Suitable anodization methods are known in the art. For example, the constant porosity may be in the range of 45 - 70% and the current density may be in the range of 30 - 100 mA/cm^2. The electrolyte may be a 49% HF plus a surfactant such as ethanol.

[0022] Alternatively, a two current step sequence may be used to form an upper PS layer 106a and a lower PS layer 106b, as shown in FIG. 3I. PS layer 106a may have a thickness in the range of 0.2 - 1 μm and a porosity in the range of 25 - 40%. This may be accomplished using a current density in the range of 1 - 5 mA/cm^2. PS layer 106b may then have a thickness in the range of 10 μm to perhaps the wafer thickness thick and a higher porosity in the range of 45 - 70%. This may be accomplished using a current density in the range of 30 - 100 mA/cm^2. The electrolyte may be the same in both cases: 49% HF + surfactant such as ethanol (approximately 50% solution of each).

[0023] If p- wafers are used, the anodization process may be performed while illuminating the back side of the wafers with above bandgap optical radiation. Exposing the wafers to light will reduce the resistivity of the Si.

[0024] After the formation of PS region 106, an polymetal dielectric (PMD) 120 is deposited. PMD 120 typically comprises a PECVD TEOS. However, other PMD materials known in the art may alternatively be used as well as silicon nitride or SiC. If SiC is used , the process should also be a PECVD using trimethylsilane (or other organosilicon gas) and a Ar or He carrier gas @ ~5 Torr (gas flow 500-5000 sccm), RF power density ~2 W/cm^2 (13.56 MHz). Substrate temp 200 - 500 °C.

[0025] The PMD 120 is then patterned and a contact etch is performed to etch through the PMD 120, SiC masking layer 104 and the optional oxide layer if present down to the silicide 110, as shown in FIG. 3J. A multistep etch is preferably used because an etch that will remove both SiC and SiO_2 will probably have poor selectivity between the dielectrics and the silicide, and most likely cut into the silicide. Without the multistep etch, poor process control may result.

[0026] Processing then continues to form metal interconnect layers and any passive components. In order to be isolated from the substrate, these passive components would be formed over PS regions 106.

[0027] A process for forming selective PS areas according to a second embodiment will now be discussed in further detail. In this embodiment, the SiC masking layer 104 is deposited after the transistor silicide process and is removed from the regions through which contacts will be made. As in the first embodiment, device is processed through isolation regions 108 and transistor 102 formation. Transistors 102 are fabricated through silicide 110 formation and anneal (Ti or W). Isolation regions 108 are shown as field oxide regions. However, there may alternatively be another type of isolation such as shallow trench isolation.

[0028] First, an oxide layer 111 is deposited as shown in FIG. 4A. In this embodiment, this oxide layer is not optional and must be present for the removal of SiC later in the process. This oxide layer may be deposited by, for example, PETEOS or LPCVD TEOS to a thickness on the order of 1000Å.

[0029] Next, a resist layer 112 is formed over the surface. The resist layer 112 is patterned as shown in FIG. 4B to expose an area 114 of isolation region 108. Area 114 is located over the desired PS site. Then, the oxide of isolation regions 108 is etched leaving sloped sidewalls on the order of 45°, as shown in FIG. 4C. This may, for example, be accomplished in one of the following two ways: (1) isotropic plasma etch using CF_4/O_2 or its equivalent or (2) HF deglaze. Resist layer 112 is then removed using standard ash/cleanup processes.

[0030] If p+ wafers with a p-epi layer are used, a p+ implant/diffusion step is needed prior to transistor formation to convert the p- epi to p+ resistivity on the order of 0.01 Ω-cm where porous silicon is desired. An deglaze/oxide etch may subsequently be performed to removed the dopant contaminated oxide and a pad oxide may be regrown to a thickness on the order of 100-500Å.

[0031] Referring to FIG. 4D, a masking layer 104 of a-SiC:H is deposited over the structure. Layer 104 may typically have a thickness in the range of 1000Å to 5000Å. The following process may be used: PECVD using trimethylsilane and Ar or He as carrier gas. The pressure may be on the order of 5 Torr. The gas flow may be in the range of 500-2000 sccm. RF power density may be on the order of 2 W/cm^2 (13.56 MHz). The

substrate temperature may be in the range of 200 - 500 °C. If desired, a double deposition step (using the same conditions) may be used to reduce defects.

[0032] Next, a second resist mask 116 is formed over the SiC masking layer 104. Second resist mask 116 exposes a portion 118 of SiC masking layer 104 approximately in the center of where the PS region is desired, as shown in FIG. 4E. The exposed portion 118 is significantly smaller than the width of the desired PS region. The relationship between the size of portion 118 and the desired PS region is optimized based on the PS formation process parameters.

[0033] The exposed portion 118 of SiC masking layer 104 is removed. Methods for removing SiC are known in the art. The following are some exemplary methods for removing portion 118 of SiC masking layer 104. (1) Cl_2 based etch [Selectivity of the etch, with this gas, down to the oxide should not be an issue. Removal rate for SiC relative to SiO_2 of 10:1 has been achieved.] using a chamber pressure: ~300 mTorr (gas flow 10 - 50 sccm) and RF Power density ~0.5 - 1 W/cm^2 (13.56 MHz); (2) $CF_4/O_2/H_2$ based etch using an O_2 fraction 0 - 90%, H_2 flow 0 - 20 sccm, (fluorinated-O_2 gas flow 10 - 50 sccm), chamber pressure; ~10 - 50 mTorr, and RF Power density ~0.5 - 1 W/cm^2 (13.56 MHz); (3) $SF_6/O_2/H_2$ based etch using O_2 fraction 0 - 90%, H_2 flow 0 - 20 sccm, (fluorinated-O_2 gas flow 10 - 50 sccm), chamber pressure; ~10 - 50 mTorr, and RF Power density ~0.5 - 1 W/cm^2 (13.56 MHz); and (4) $CHF_3/CF_4/Ar/O_2/H_2$ based etch using an O_2 fraction 0 - 50%, H_2 flow 0 - 100 sccm, (fluorinated-Ar gas flow 50 - 200 sccm), chamber pressure: ~10 - 50 mTorr, and RF Power density ~0.5 - 1 W/cm^2 (13.56 MHz). Second resist layer 118 is then removed.

[0034] Next, the PS regions 106 are formed by anodization, as shown in FIG. 4F. The thickness of PS region 106 may vary between 10 μm and perhaps the wafer thickness, depending on the application. Typically, PS region 106 may be in the range of 10 - 200 μm. The constant porosity may be in the range of 45 - 70% and the current density may be in the range of 30 - 100 mA/cm^2. The electrolyte may be a 49% HF plus a surfactant such as ethanol.

[0035] Alternatively, a two current step sequence may be used to form an upper PS layer 106a and a lower PS layer 106b as in the first embodiment. PS layer 106a may have a thickness in the range of 0.2 - 1 μm and a porosity in the range of 25 - 40%. This may be accomplished using a current density in the range of 1 - 5 mA/cm^2. PS layer 106b may then have a thickness in the range of 10 μm to perhaps the wafer thickness thick and a higher porosity in the range of 45 - 70%. This may be accomplished using a current density in the range of 30 - 100 mA/cm^2. The electrolyte may be the same in both cases: 49% HF + surfactant such as ethanol (approximately 50% solution of each).

[0036] If p- wafers are used, the anodization process may be performed while illuminating the back side of the wafers with above bandgap optical radiation. Exposing the wafers to light will reduce the resistivity of the Si.

[0037] After the formation of PS region 106, the following optional sequence may be performed. First, a capping layer 122 may be deposited over the SiC masking layer 104, as shown in FIG. 4G. The capping layer may comprise SiC or silicon nitride and have a thickness on the order of 1500Å. If SiC is used, the same deposition process should be used as earlier in the process. Second, a third resist mask 124 is then formed over capping layer 122 leaving the areas anodized covered and exposing the remaining areas.

[0038] Whether or not the above optional sequence is performed, the SiC masking layer 104 and capping layer 122 if present are etched stopping on oxide layer 111. If the optional third resist mask 124 is used, portions of SiC masking layer 104 will remain over the PS regions 106. Otherwise, the entirety of SiC masking layer 104 is removed. If present, the third resist mask is removed.

[0039] Next, PMD 120 is deposited. PMD 120 typically comprises a PECVD TEOS. However, other PMD materials known in the art may alternatively be used. The PMD 120 is then patterned and a contact etch is performed to etch through the PMD 120 and oxide layer 111 down to the silicide 110 as shown in FIG. 4H. In this embodiment a multi-step etch to account for removing SiC is not required. Processing then continues to form metal interconnect layers and any passive components. In order to be isolated from the substrate, these passive components would be formed over PS regions 106.

[0040] While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. For example, while the low temperature aspect of the invention is especially advantageous after transistor fabrication, the process according to the invention may alternatively be performed (in whole or part) prior to transistor fabrication. A p+ diffusion of boron or similar dopant may be performed prior to the transistor formation to convert the p-epi to p+ w/resistivity on the order of 0.01Ω-cm. If necessary, a deglaze to remove the boron or similar dopant contaminated oxide is then performed and a pad oxide is re-grown to a thickness on the order of 100-500Å.

Claims

1. A method of fabricating a porous silicon region in a substrate having a isolation region formed therein, comprising the steps of:

   patterning and etching said isolation region to expose a first area of said substrate;

   depositing, by plasma enhanced chemical vapor deposition using an organosilicon pre-

cursor gas, a layer of silicon carbide over said substrate including said first area, said depositing step occurring at a temperature in the range of 200-500°C;

patterning and etching said silicon carbide layer to expose a second area of said substrate within said first area; and

forming a porous silicon region in said first area using an HF electrolyte, wherein said silicon carbide layer protects said transistor from the HF electrolyte.

2. The method of Claim 1, wherein said depositing step comprises depositing by PECUD using an organosilicon precursor gas that comprises trimethylsilane.

3. The method of Claim 1 or Claim 2, wherein said step of patterning and etching said isolation region forms angled sidewalls having a slope substantially on the order of 45°.

4. The method of any preceding claim, wherein said step of depositing a silicon carbide layer comprises depositing a silicon carbide layer having a thickness in the range of 1000 - 5000 Å.

5. The method of any preceding claim, further comprising performing said step of depositing said silicon carbide layer using following processing parameters: a carrier gas supplied at a pressure on the order of 4 Torr and a gas flow in the range of 500-5000 sccm, and a RF power density on the order of 2W/cm^2 at a frequency on the order of 13.56 MHz.

6. The method of any Claims 1 to 5, wherein said step of patterning and etching said silicon carbide layer comprises the step of etching in chlorine with a chamber pressure on the order of 300 mTorr, a gas flow in the range of 10-50 sccm, and a RF power density in the range of 0.5 - 1 W/cm^2 at a frequency on the order of 13.56 MHz

7. The method of any of Claims 1 to 5, wherein said step of patterning and etching said silicon carbide layer comprises the step of etching in $CF_4/O_2/H_2$ with a chamber pressure on the order of 10 - 50 mTorr, a gas flow for H_2 in the range of 0-20 sccm and for fluorinated oxygen in the range of 10 - 50 sccm, and a RF power density in the range of 0.5 - 1 W/cm^2 at a frequency on the order of 13.56 MHZ.

8. The method of any of Claims 1 to 5, wherein said step of patterning and etching said silicon carbide layer comprises the step of etching in $SF_6/O_2/H_2$ with a chamber pressure on the order of 10 - 50 mTorr, a gas flow for H_2 in the range of 0-20 sccm and for fluorinated oxygen in the range of 10 - 50 sccm, and a RF power density in the range of 0.5 - 1 W/cm^2 at a frequency on the order of 13.56 MHZ.

9. The method of any Claims 1 to 5, wherein said step of patterning and etching said silicon carbide layer comprises the step of etching in $CHF_3/CF_4/Ar/O_2/H_2$ with a chamber pressure on the order of 10 - 50 mTorr, a gas flow for H_2 in the range of 0-100 sccm and for fluorinated argon in the range of 50 - 200 sccm, and a RF power density in the range of 0.5 - 1 W/cm^2 at a frequency on the order of 13.56 MHZ.

10. The method of any preceding claim, wherein said step of forming said porous silicon region comprises anodization in a HF electrolyte and a current density in the range of 30 - 100 mA/cm^2.

11. A substrate having a porous silicon region formed in an isolation region thereof, said porous silicon region being formed according to the method of any of Claims 1 to 10.

12. A semiconductor device comprising a substrate having a porous silicon region formed in an isolation region thereof, said porous silicon region being formed according to the method of any of Claims 1 to 10.

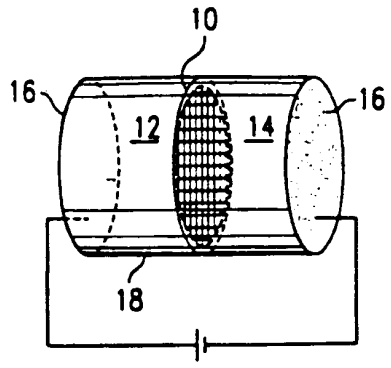

FIG. 1

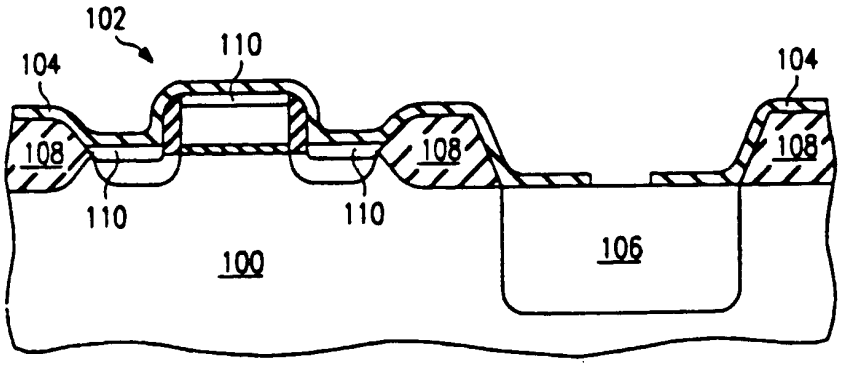

FIG. 2

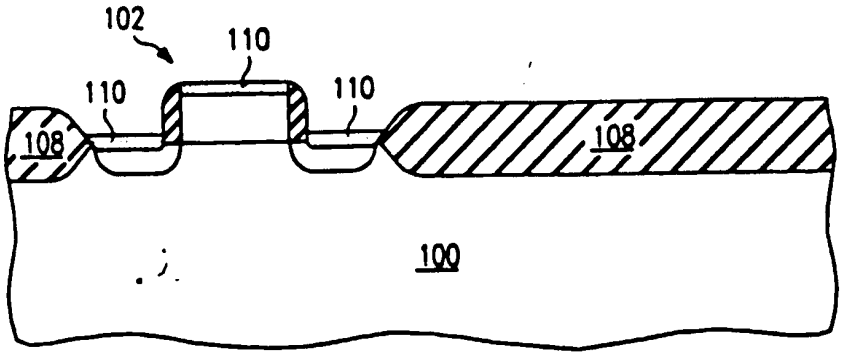

FIG. 3A

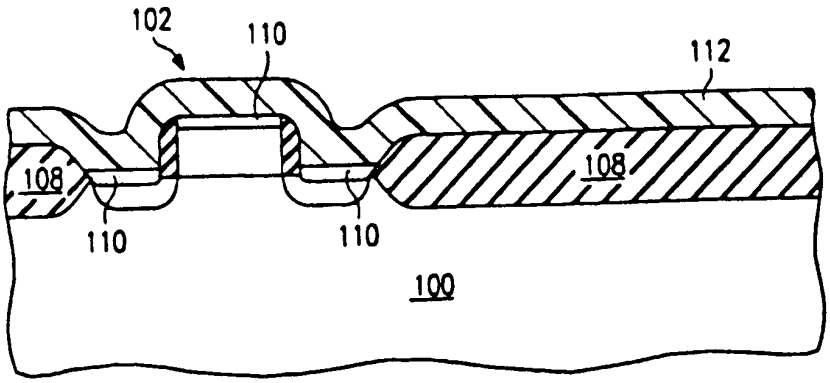

FIG. 3B

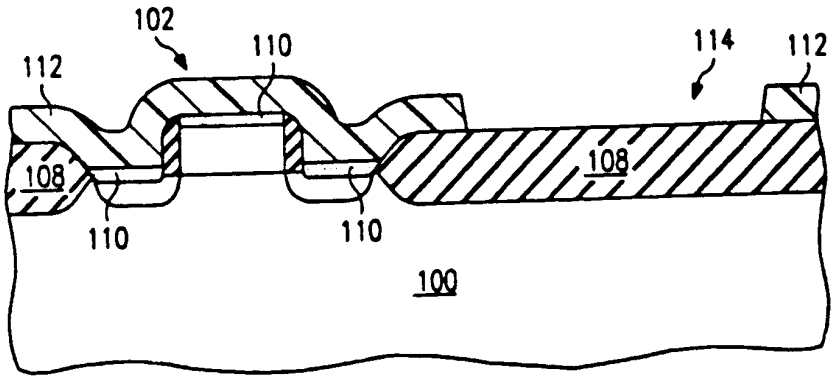

FIG. 3C

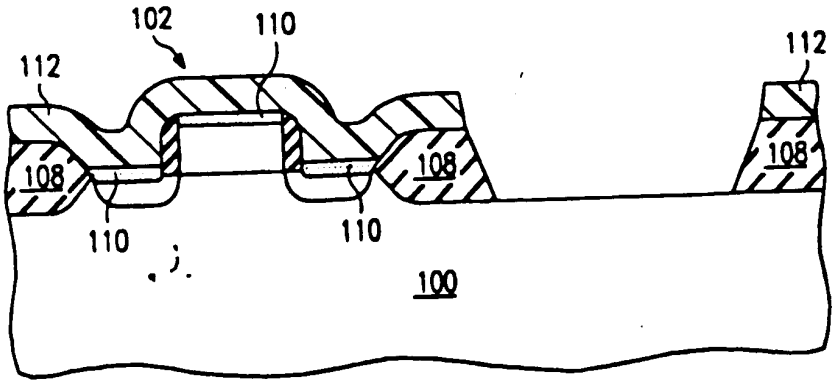

FIG. 3D

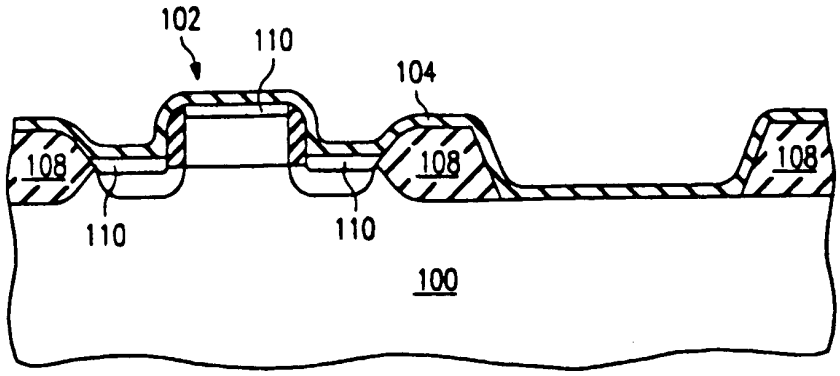

FIG. 3E

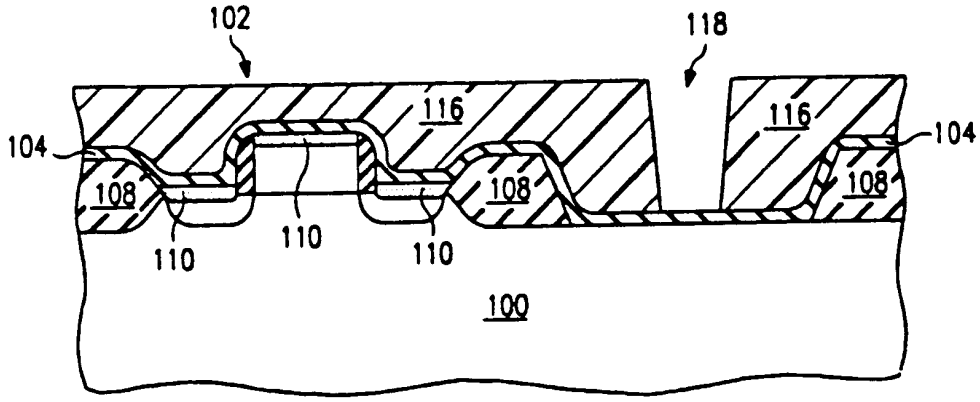

FIG. 3F

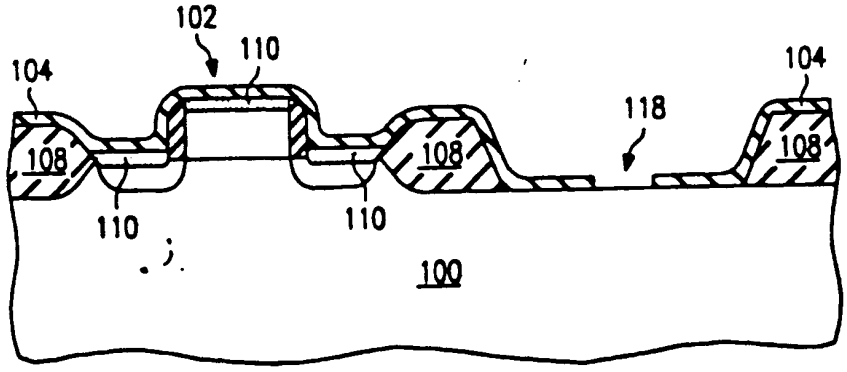

FIG. 3G

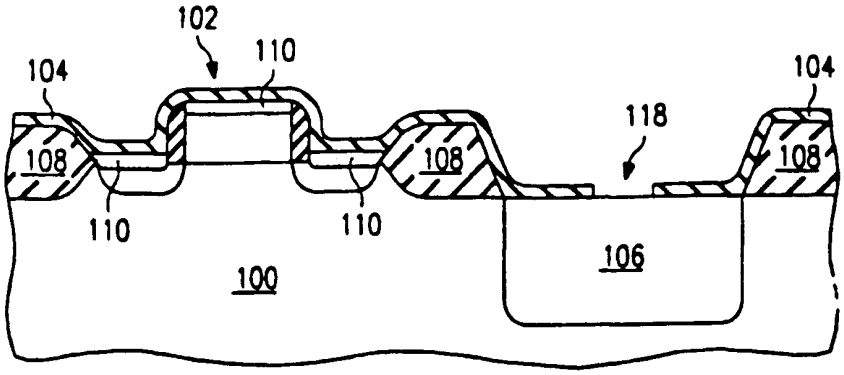

FIG. 3H

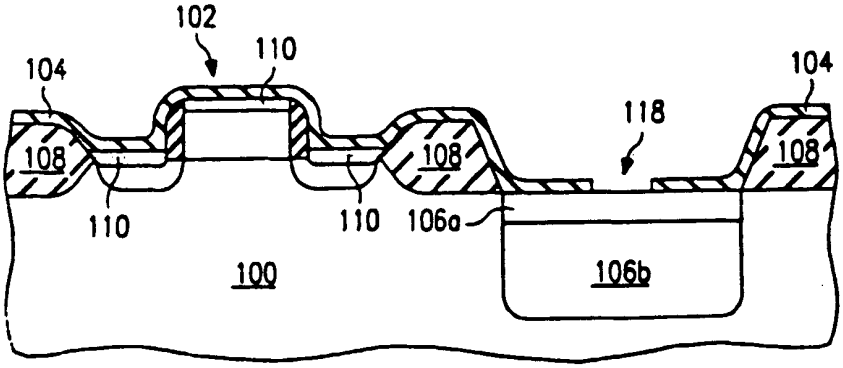

FIG. 3I

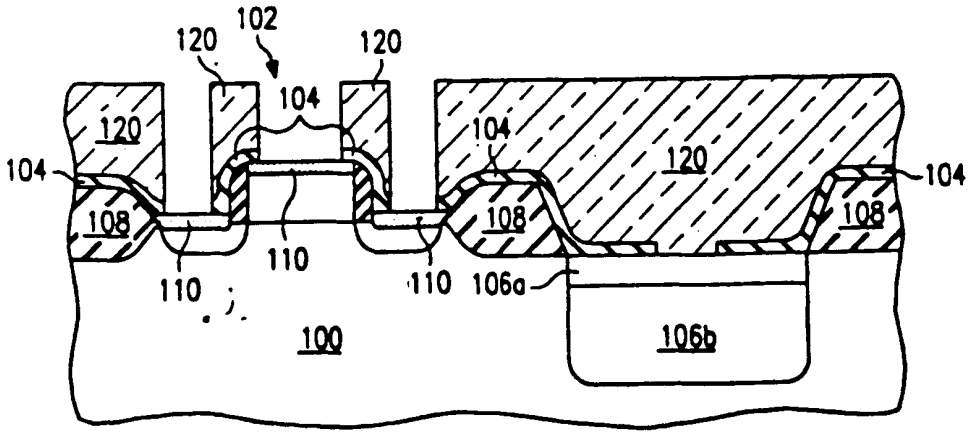

FIG. 3J

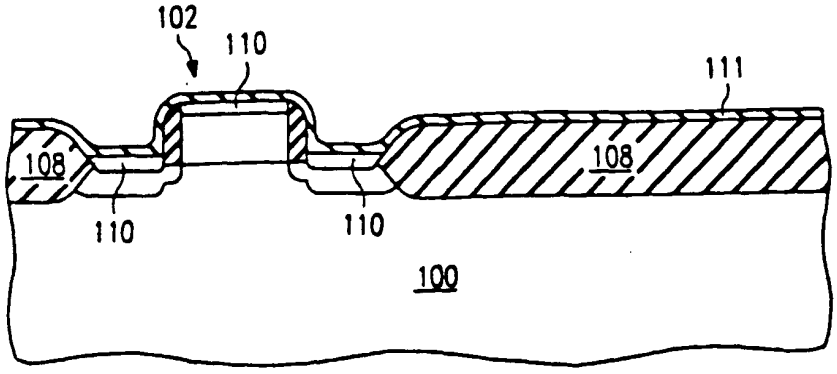

FIG. 4A

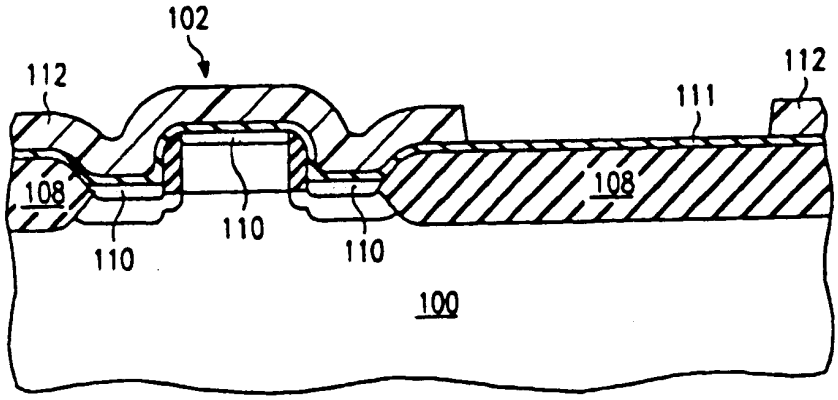

FIG. 4B

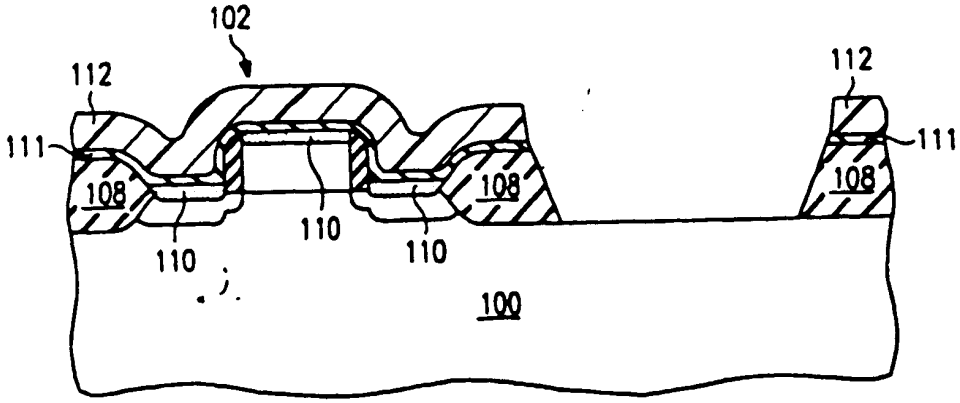

FIG. 4C

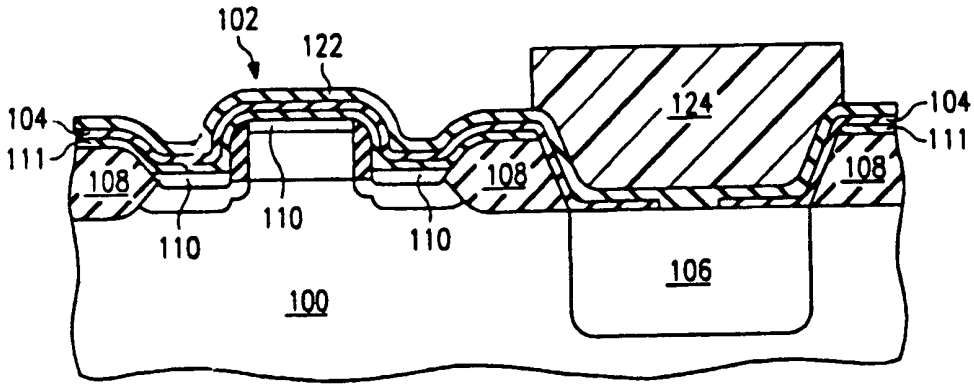
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FIG. 4G

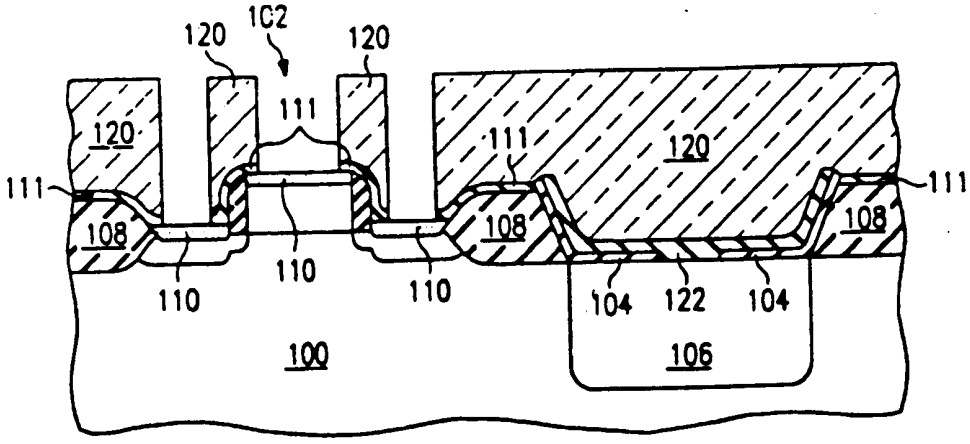
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FIG. 4H